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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,439	11/16/2001	Nicholas E. Aneshansley	2070.005800/P6758	6089

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,439	ANESHANSLEY, NICHOLAS E.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10,11,14-16,18,20-30 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8,10,11,14-16,18,20-30 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-8, 10, 11, 14-16, 18, 20-30 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by DROGICHEN (U.S. Patent 6,571,360).

As to claim 1, DROGICHEN teaches a method comprising: processing tasks associated with at least one processor (col. 5, lines 57-58), wherein the processor comprises at least one cache memory (contents of memory) having data stored therein (col. 5, lines 57-58); transferring at least a portion of the data of the cache memory to another location (via migrating the contents of memory to other boards) (col. 5, lines 57-58); and removing a board including the processor and the cache memory from a system in response to transferring at least the portion of the data from the cache memory to another location, while the system is in operation (The dynamic reconfiguration can be performed while the computer system is in operation and the processors are taken offline and later physically removed from the system) (col. 5, line 47 – col. 6, line 5). It is inherent from the system of DROGICHEN that a signal must be used between the cited steps to indicate when to perform the second step, i.e. when to

thereby remove the processor from the system. If not, the invention would never perform the first step because the processor would be physically removed before any information is rerouted, stored, or locked and thereby destroy all of the tasks that were executing on the processor being removed. The invention prevents a faulty I/O board from causing errors in the isolated portion of the system, thereby shielding ongoing user applications and preventing any system crashes that might result from propagation of incorrect signals from the faulty I/O board (col. 3, lines 22-26). If the second step was performed prior to or before the first step was performed, other user applications using or invoking data on the faulty processor would thereby crash, because their routes were not rerouted, etc. which is precisely what the first step of the detaching operation would do to avoid the crash. Therefore, the first step of the detaching operation is fully performed and the second operation, i.e. the physically removal of the processor is subsequently performed. In order for one to know when to physically remove a processor, a signal or indication of the first step being completely performed would have to be received. This is shown by after finishing the substeps of the first step of the detaching operation, the processor is taken offline. The marking of the processor offline, would be a signal that it is safe to remove the processor. Therefore, the limitation of sending/receiving an acknowledgement signal indicating when it is safe to remove the board from the system is inherent to the teachings of DROGICHEN by taking the processor offline.

As to claim 2, DROGICHEN teaches transferring at least the portion of the data of the cache memory to another location comprises transferring at least the portion of the data of the cache memory to non-cache memory in the system (col. 5, line 57 – col. 6, line 5).

As to claim 3, DROGICHEN teaches a domain defined therein, wherein transferring at least the portion of the data comprises transferring at least the portion of the data of the cache memory of the domain to non-cache memory of the domain in the system (col. 5, line 57 – col. 6, line 5).

As to claim 5, DROGICHEN teaches removing the board comprises removing the board from the domain in the system (col. 5, line 57 – col. 6, line 5).

As to claim 11, DROGICHEN teaches an apparatus, comprising: at least one processor (processor / board) to execute one or more assigned tasks wherein the processor includes at least one associated cache memory element having data stored therein (process execution) (col. 5, lines 57-58); and an interface to couple the apparatus to a system, wherein the apparatus is adapted to be removed from the system in response to executing the one or more assigned tasks and in response to transferring a portion of the data of the cache memory to a non-cache memory external to the apparatus, while the system is in operation (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into

the system dynamically) (col. 5, lines 40 – col. 6, line 5). It is inherent from the system of DROGICHEN that a signal must be used between the cited steps to indicate when to perform the second step, i.e. when to thereby remove the processor from the system. If not, the invention would never perform the first step because the processor would be physically removed before any information is rerouted, stored, or locked and thereby destroy all of the tasks that were executing on the processor being removed. The invention prevents a faulty I/O board from causing errors in the isolated portion of the system, thereby shielding ongoing user applications and preventing any system crashes that might result from propagation of incorrect signals from the faulty I/O board (col. 3, lines 22-26). If the second step was performed prior to or before the first step was performed, other user applications using or invoking data on the faulty processor would thereby crash, because their routes were not rerouted, etc. which is precisely what the first step of the detaching operation would do to avoid the crash. Therefore, the first step of the detaching operation is fully performed and the second operation, i.e. the physically removal of the processor is subsequently performed. In order for one to know when to physically remove a processor, a signal or indication of the first step being completely performed would have to be received. This is shown by after finishing the substeps of the first step of the detaching operation, the processor is taken offline. The marking of the processor offline, would be a signal that it is safe to remove the processor. Therefore, the limitation of sending/receiving an acknowledgement signal indicating when it is safe to remove the board from the system is inherent to the teachings of DROGICHEN by taking the processor offline.

As to claim 16, DROGICHEN teaches a system comprising: an interface adapted to receive a first processor (processor / I/O board) and an associated cache memory; a control unit adapted to cause at least a portion of the contents of the associated cache memory to be transferred to a second memory location (migrate contents of memory to other boards) and, in response to the transfer, the first processor to be removed from a domain of the system, while the system is in operation (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5). DROGHICHEN teaches the detaching operation migrating process execution, network and I/O connections to other boards, flushing memory to disk and remapping kernel memory to other board, locking free pages to prevent further use, switching network devices and file systems to alternate paths, i.e. to other boards, and taking the processors offline. The detaching operation then allows for the physical removal of the processor from the system. It is inherent to the teachings of DROGICHEN that if the processor is not physically attached to the system, additional task can never be assigned to it. Hence, if one physically removes a processor from a computer system such that it is totally independent and separate from the system, the computer system can never assign task to the processor, since the processor is not attached in no form, to the computer system. Therefore, DROGHICHEN teaches the stopping of assignment of tasks to the first processor by another processor or a control unit because the processor is no longer connected to the

computer system or the processor for receiving a task. Therefore, it would be impossible to assign a task to an unconnected processor by another processor or a control unit.

As to claim 23, DROGICHEN teaches a system comprising: a first board having a memory element (microprocessor and I/O boards); a second board having a processor an only a cache memory element (other boards), wherein the processor is adapted to execute one or more current tasks (process execution); a control unit adapted to receive an indication to dynamically remove the second board from a domain of the system, wherein the control unit, in response to receiving the indication, is adapted to process at least one current tasks associated with the processor and transfer at least a portion of data stored in the cache memory on the second board to the memory element of the first board (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5). DROGHICHEN teaches the detaching operation migrating process execution, network and I/O connections to other boards, flushing memory to disk and remapping kernel memory to other board, locking free pages to prevent further use, switching network devices and file systems to alternate paths, i.e. to other boards, and taking the processors offline. The detaching operation then allows for the physical removal of the processor from the system. It is inherent to the teachings of DROGICHEN that if the processor is not physically attached to the system, additional

task can never be assigned to it. Hence, if one physically removes a processor from a computer system such that it is totally independent and separate from the system, the computer system can never assign task to the processor, since the processor is not attached in no form, to the computer system. Therefore, DROGHICHEN teaches the stopping of assignment of tasks to the first processor by another processor or a control unit because the processor is no longer connected to the computer system or the processor for receiving a task. Therefore, it would be impossible to assign a task to an unconnected processor by another processor or a control unit.

As to claim 26, DROGICHEN teaches an apparatus, comprising: at least two processors (microprocessor board / control boards / I/O board), wherein each processor has at least one associated cache memory but no non-cache memory (col. 5, lines 57-58); an address repeater coupled to the two processors, wherein the address repeater is adapted to receive at least one data request and to provide the request to at least one of the two processors (via the system interconnect bus) (col. 4, lines 5-20); a data crossbar (centerplane) (col. 3, lines 64-66); a dual CPU data switch (control and arbitration subsystems) coupled to the two processor and the crossbar, wherein the dual CPU data switch is adapted to provide data from at least one of the cache memories of the two processor to the data crossbar in response to the received data request; (via the centerplane containing two symmetrical sides that can each mount multiple expander boards and a system control board wherein communication is communicated through the interconnect bus and supported by control and arbitration

subsystems) (col. 4, lines 1-20); and a data controller coupled to the network wherein the data controller is adapted to indicate to the network where to send the requested data (via the system administrator using the system controller to dynamic configure various microprocessor and I/O boards into the system dynamically by removing and attaching processors and I/O boards) (col. 5, lines 40 – col. 6, line 5).

As to claims 28-32, reference is made to an article that corresponds to the method of claims 1-5 and is therefore met by the rejection of claims 1-5 above.

As to claim 6, DROGICHEN teaches processing the tasks associated with the at least one processor comprises stopping new tasks from being assigned to the processor (via taking the processor offline) (col. 5, lines 47-col. 6, line 5).

As to claim 7, DROGHICHEN teaches processing the tasks comprises allowing the processor to substantially complete current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 8, DROGHICHEN teaches processing the tasks comprises flushing the current state of the processor (via the operating system flushes all pageable memory to disk) (col. 5, line 47 – col. 6, line 5).

As to claim 10, DROGHICHEN teaches transferring at least a portion of the data comprises transferring all of the data stored in the cache memory (via migrating the contents of memory) (col. 5, line 47 – col. 6, line 5).

As to claim 14, DROGHICHEN teaches the portion of the data comprises all the data stored in the cache memory (col. 5, line 47- col. 6, line 5).

As to claim 15, DROGHICHEN teaches the processor is adapted to transmit a signal to the system when the processor has substantially completed the one or more assigned task via placing the processor in an offline state such that the centerplane hardware isolates the component from is previous system to available to be physically removed) (col. 5, line 47 – col. 6, line 5).

As to claim 18, DROGHICHEN teaches the second memory location comprises a non-cache memory in the domain (memory) (col. 5, line 47 – col. 6, line 5).

As to claim 20, DROGHICHEN teaches the second processor is further adapted to allow the first processor to substantially complete the current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 21, DROGHICHEN teaches the second processor is adapted to reassign current tasks (via migrating process execution) (col. 5, line 47 – col. 6, line 5).

As to claim 22, DROGHICHEN teaches the second processor is adapted to flush the current state of the first processor (via the operating system flushes all pageable memory to disk) (col. 5, line 47 – col. 6, line 5).

As to claim 24, DROGHICHEN teaches the control unit is adapted to allow the processor on the second board to complete the one or more current tasks (via performing all other operating system task before taking the processor offline) (col. 5, lines 47 – col. 6, line 5).

As to claim 25, DROGHICHEN teaches wherein the control unit is adapted to reassign at least one of the current tasks associated with the processor of the second board to the processor of the first board (via migrating process execution) (col. 5, line 47 – col. 6, line 5).

As to claim 27, DROGHICHEN teaches at least one of the processors is adapted to send data address requests through the address repeater and receive the requested data through the data crossbar and dual CPU data switch (via the centerplane containing two symmetrical sides that can each mount multiple expander boards and a

system control board wherein communication is communicated through the interconnect bus and supported by control and arbitration subsystems) (col. 4, lines 1-20).

Response to Arguments

3. Applicant's arguments filed January 11, 2006 have been fully considered but they are not persuasive. Applicant argues that the teachings of DROGICHEN does not teach the sending of an acknowledgement signal indicating that it is safe to remove the board from the system. The examiner disagrees. DROGICHEN teaches a two step operation for detaching a processor board from the computer system. The first step involves the operating system flushing all pageable memory to disk and remaps kernel memory to other boards, locks free pages to prevent further use, switches network devices and file systems to alternative paths, and finally takes the processors offline. The second step involves the isolation of the component from its previous system domain wherein in thereby the processor becomes available for physical removal from the system (col. 5, line 59 – col. 6, line 5). It is inherent from the system of DROGICHEN that an signal must be used between the cited steps to indicate when to perform the second step, i.e. when to thereby remove the processor from the system. If not, the invention would never perform the first step because the processor would be physically removed before any information is rerouted, stored, or locked and thereby destroy all of the tasks that were executing on the processor being removed. The invention prevents a faulty I/O board from causing errors in the isolated portion of the system, thereby shielding ongoing user applications and preventing any system crashes

that might result from propagation of incorrect signals from the faulty I/O board (col. 3, lines 22-26). If the second step was performed prior to or before the first step was performed, other user applications using or invoking data on the faulty processor would thereby crash, because their routes were not rerouted, etc. which is precisely what the first step of the detaching operation would do to avoid the crash. Therefore, the first step of the detaching operation is fully performed and the second operation, i.e. the physically removal of the processor is subsequently performed. In order for one to know when to physically remove a processor, a signal or indication of the first step being completely performed would have to be received, therefore, the limitation of sending/receiving an acknowledgement signal indicating when it is safe to remove the board from the system is inherent to the teachings of DROGICHEN. In addition, the examiner can cite numerous references where this inherent feature would have to be performed. See for instance, U.S. Patents 6,378,027; 6,282,596; 5,202,965; and 4,606,024. In all the references, it is inherent to disconnecting processors to a computer system that the task/data is stored onto another memory device and the redistributing or rerouting of tasks to other processors are performed before the processor is physically removed. When the data is restored and the task/data rerouted, the system signals that the processor can be removed. The cited references are examples of this inherent feature of signaling the physically removal of processors from a computer system. DROGHICHEN as used in the 35 U.S.C. 102 rejections, inherently has this capability in order to physically remove processors without crashing the computer system.

Applicant then argues that DROGICHEN does not teach or suggest the second processor is adapted to stop the assignment of additional tasks to the first processor. The examiner disagrees. DROGHICHEN teaches the detaching operation migrating process execution, network and I/O connections to other boards, flushing memory to disk and remapping kernel memory to other board, locking free pages to prevent further use, switching network devices and file systems to alternate paths, i.e. to other boards, and taking the processors offline. The detaching operation then allows for the physical removal of the processor from the system. It is inherent to the teachings of DROGICHEN that if the processor is not physically attached to the system, additional task can never be assigned to it. Hence, if one physically removes a processor from a computer system such that it is totally independent and separate from the system, the computer system can never assign task to the processor, since the processor is not attached in no form, to the computer system. Therefore, DROGHICHEN teaches the stopping of assignment of tasks to the first processor by another processor or a control unit because the processor is no longer connected to the computer system or the processor for receiving a task. Therefore, it would be impossible to assign a task to an unconnected processor by another processor or a control unit.

4. In regards to claim 26, Applicant makes a general allegation that DROGICHEN does not teach the address repeater, a dual CPU data switch or the functioning between such. The examiner has provided a rationale of how the teachings of DROGICHEN teach all of the limitations. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a

patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. In essence, Applicant provides no rational of how the Examiner's interpretation is not met by the claim language as disclosed. Therefore, the examiner refers to the interpretation above in showing that all the claim language is met and maintains the rejection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

March 27, 2006